Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Amended) A method of forming multiple gate insulator layers on semiconductor substrate having a core region and an input/output (I/O) region, the method comprising the steps of:

forming a first insulator layer over a silicon containing semiconductor substrate;

removing said first insulator layer from ~~a second portion~~ the I/O region of said semiconductor substrate, resulting in a first gate insulator layer having a first insulator thickness, located on ~~a first portion~~ the core region of said semiconductor substrate;

performing a pre-clean procedure, wherein said pre-clean procedure can remove a native oxide from said semiconductor substrate; and

selectively forming a second gate insulator layer, having a second insulator thickness, on said ~~second portion~~ I/O region of said semiconductor substrate.

2. (Original) The method of claim 1, wherein a first pre-clean procedure is performed in a buffered hydrofluoric (BHF), acid solution, comprised of HF in ammonium fluoride, performed prior to formation of said first insulator layer.

3. (Amended) The method of claim ~~1~~ 2, wherein said first pre-clean procedure is a wet procedure, performed in a dilute HF acid solution, comprised of HF in de-ionized water.

4. (Amended) The method of claim ~~1~~ 2, wherein said first pre-clean procedure is a dry procedure, performed via use of HF vapors.

5. (Amended) The method of claim 1, wherein said first insulator layer is a silicon nitride layer, comprised with said first insulator thickness ~~between~~ is less than about 30 ~~to 80~~ Angstroms and said second gate insulator layer is a silicon dioxide layer with said second gate insulator layer thickness greater than about 30 Angstroms.

6. (Original) The method of claim 1, wherein said first insulator layer is a silicon nitride layer, obtained via direct plasma nitridization on said semiconductor substrate.

7. (Original) The method of claim 1, wherein said first insulator layer is a silicon nitride layer, obtained via direct thermal nitridization procedures on said semiconductor substrate.

8. (Original) The method of claim 1, wherein said first insulator layer is a silicon nitride layer, obtained via rapid thermal chemical vapor deposition (RTCVD), procedures.

9. (Original) The method of claim 1, wherein said first insulator layer is a silicon nitride layer, obtained via remote plasma enhanced chemical vapor deposition (RPCVD), procedures.

10. (Original) The method of claim 1, wherein said first insulator layer is a silicon nitride layer, obtained via atomic layer chemical vapor deposition (ALCVD), procedures.

11. (Original) The method of claim 1, wherein said first insulator layer is removed from said second portion of said semiconductor substrate using a hot phosphoric acid solution as an etchant for said first insulator layer.

12. (Original) The method of claim 1, wherein said first insulator layer is removed from said second portion of said semiconductor substrate via dry etch procedures using CF_4 or $C1_2$ as an etchant for said first insulator layer.

13. (Original) The method of claim 1, wherein said pre-clean procedure is a wet procedure, performed in a buffered hydrofluoric (BI-IF), acid solution, comprised of HF in ammonium fluoride.

14. (Original) The method of claim 1, wherein said pre-clean procedure is a wet procedure, performed in a dilute HF acid solution, comprised of HF in de-ionized water.

15 (Original) The method of claim 1, wherein said pre-clean procedure is a dry procedure, performed via use of HF vapors.

16. (Original) The method of claim 1, wherein said second gate insulator layer is a silicon dioxide layer, comprised with said second insulator thickness between about 30 to 80 Angstroms.

17. (Original) The method of claim 1, wherein said second gate insulator layer is formed via a thermal oxidation procedure, performed in an oxygen content ambient.

18. (Original) The method of claim 1, wherein said second gate insulator layer is formed via a plasma oxidation procedure, performed in an oxygen content ambient.

19. (Original) The method of claim 1, wherein said first gate insulator layer is annealed during formation of said second gate insulator layer.

20. (Amended) A method of forming multiple thickness gate insulator layers on a silicon containing substrate, featuring a hydrofluoric (HF), pre-clean procedure performed prior to formation of each gate insulator layer, comprising the steps of:

forming a first dielectric layer over said silicon containing substrate;

selectively removing said first dielectric layer from a second portion of said silicon containing substrate resulting in a first dielectric gate insulator layer, having a first insulator thickness, located on a first portion of said silicon containing substrate; and

performing an oxidation procedure to form a second dielectric gate insulator layer, having a second insulator thickness greater than the first thickness, on said second portion of said silicon containing substrate, wherein the removal rate of said second dielectric gate insulator layer is higher than the removal rate of said first dielectric layer using a prescribed etchant.

21. (Original) The method of claim 20, wherein a first HF pre-clean procedure is performed prior to formation of said first dielectric layer, performed in a buffered hydrofluoric (BHF), acid solution, comprised of HF in ammonium fluoride, or performed in a dilute HF acid solution, comprised of HF in de-ionized water.

22. (Original) The method of claim 20, wherein a first HF based pre-clean procedure is performed prior to formation of said first dielectric layer via use of HF vapors.

23. (Original) The method of claim 20, wherein said first dielectric layer is a silicon nitride layer, obtained at a thickness between about 5 to 30 Angstroms, via a direct plasma nitridization

procedure, performed on said silicon containing substrate.

24. (Original) The method of claim 20, wherein said first dielectric layer is a silicon nitride layer, obtained at a thickness between about 5 to 30 Angstroms, via direct thermal nitridization on said silicon containing substrate.

25. (Original) The method of claim 20, wherein said first dielectric layer is a silicon nitride layer, obtained at a thickness between about 5 to 30 Angstroms, via rapid thermal chemical vapor deposition (RTCVD), procedures, or performed via remote plasma enhanced chemical vapor deposition (RPCVD), procedures, performed using silane or disilane, and ammonia as reactants.

26. (Original) The method of claim 20, wherein said first dielectric layer is a silicon nitride layer; obtained at a thickness between about 5 to 30 Angstroms, via atomic layer chemical vapor deposition (ALCVD), procedures

27. (Original) The method of claim 20, wherein said first dielectric layer is selectively removed from said second portion of said semiconductor substrate using a hot phosphoric acid solution as an etchant.

28. (Original) The method of claim 20, wherein said first dielectric layer is selectively removed from said second portion of said semiconductor substrate via dry etch procedures using CF_4 or Cl_2 as an etchant.

29. (Original) The method of claim 20, wherein a second HF pre-clean procedure is performed prior to said oxidation procedure, in a buffered hydrofluoric (BHF), acid solution, comprised of I in ammonium fluoride, or performed in a dilute HF acid solution, comprised of HF in de-ionized water.

30. (Original) The method of claim 20, wherein said second dielectric gate insulator layer is a silicon oxide gate insulator layer is comprised with a thickness between about 30 to 80 Angstroms.

31. (Original) The method of claim 20, wherein a second HF pre-clean procedure, performed prior to said oxidation procedure, is performed via use of HF vapors.

32. (Original) The method of claim 20, wherein said oxidation procedure used to form said second dielectric gate insulator layer is a thermal oxidation procedure, performed at a temperature between about 500 to 11000 C, in an oxygen content ambient.

33. (Original) The method of claim 20, wherein said procedure used to form said second dielectric gate insulator layer is a plasma oxidation procedure, performed at a temperature between about 25 to 800° C, in an oxygen content ambient.

34. (New) A method of forming multiple gate insulator layers on semiconductor substrate comprising the sequential steps of:

performing a first pre-clean procedure, wherein said pre-clean procedure can remove a native oxide from said semiconductor substrate;

forming a first insulator layer over a silicon containing semiconductor substrate;

removing said first insulator layer from a second portion of said semiconductor substrate, resulting in a first gate insulator layer having a first insulator thickness, located on a first portion of said semiconductor substrate;

performing a second pre-clean procedure, wherein said pre-clean procedure can remove a native oxide from said semiconductor substrate; and

selectively forming a second gate insulator layer, having a second insulator thickness, on said second portion of said semiconductor substrate.